

TECHNIQUES TO REDUCE SUBSTRATE CROSS TALK
ON MIXED SIGNAL AND RF CIRCUIT DESIGN

5 Technical Field of the Invention

The present invention relates to RF isolation in integrated circuits.

Background of the Invention

10 It is well known that the general trend in semiconductor integrated circuit fabrication is to produce smaller and smaller devices so that more circuitry can be packed into less wafer real estate. This trend means that the spacing between devices of an
15 integrated circuit shrinks. As the spacing between devices shrinks, adjacent devices increasingly interact with each other, reducing performance of the integrated circuit.

The basic measurement parameter that
20 characterizes this interaction effect is called electrical isolation. If high electrical isolation, and in particular, high RF isolation, between devices of an integrated circuit can be achieved, those devices can be spaced more closely together. As a result, the die size
25 of the integrated circuit can be is minimized. Minimum size, in turn, implies smaller packaging and, thus, less space used on the application PCB Board. Also, since

wafer processing costs are nearly independent of the chip size, smaller circuits imply more die per wafer and thus a lower cost per die.

Isolation is particularly important for analog
5 integrated circuits and for analog/digital mixed
integrated circuits such as those used in wireless and
wireline communications applications. In general,
wireless communication devices use high-frequency signals
such as 900 MHz to 1900 MHz for cellular phones, and
10 higher frequencies (up to 6 GHz or more) for other
applications such as wireless LANs and fiber optic
transceivers.

RF signals at such frequencies are difficult to
generate and control. These signals also have a tendency
15 to interfere with one other because they are easily
coupled by parasitic properties present in all electronic
components, including integrated circuits. Such
undesirable parasitic effects result, for example, from
the conductive silicon substrates on which integrated
20 circuits are fabricated. Poor electrical isolation in a
receiver can lead to a local oscillator signal appearing
at the output of the receiver and being effectively
transmitted at the antenna. Wireless regulatory
authorities limit the amount of spurious signals that can

be radiated by the receiver, and limiting the amount of local oscillator radiation is important in meeting these limits.

SiO₂ trench isolation and conductive guard rings are isolation techniques that have been employed (such as with SOI processes) to isolate devices of an integrated circuit. Dielectric trench isolation structures provide lateral barriers between circuit devices. Conductive guard rings are used to enclose the area to be isolated. Both techniques isolate signals and minimize the undesired coupling that would otherwise limit performance for closely spaced adjacent circuit devices.

U.S. Patent No. 6,355,537 discloses a double ring approach where two isolation trenches (usually rectilinear) are formed around a device to be isolated. The silicon between the two isolation trenches is doped to form a conductive guard ring region, and a grounded contact is applied to the conductive guard ring region. The isolation trenches may be filled with a dielectric such as silicon oxide or oxide/polysilicon. This grounded guard ring region, the use of SOI on which the integrated circuit is formed, and the use of a high resistivity material for the substrate of the SOI greatly improves RF isolation.

However, the process disclosed in the '537 patent is primarily for thick SOI where the epitaxial layer is on the order of one micron. Moreover, the process disclosed in the '537 patent relies on an n⁺ buried layer that forms a low resistivity RF signal path. Also, the process disclosed in the '537 patent is BiCMOS (bipolar CMOS) dependent.

U.S. Patent No. 5,661,329 discloses the use of a separation groove around active regions of an integrated circuit. One disadvantage of this separation groove is that external RF power can still pass through the separation groove to the active region. Moreover, this separation groove appears to be intended primarily for yield improvement and not for RF isolation. Therefore, the '329 patent does not appear to address the problem of RF isolation and appears to show no intent to terminate electric fields created by RF power.

Summary of the Invention

According to one aspect of the present invention, an integrated circuit comprises a semiconductor substrate, a buried insulation layer over the semiconductor substrate, a semiconductor mesa over the buried insulation layer, and a guard ring

substantially surrounding the semiconductor mesa. The guard ring is in contact with the semiconductor substrate, and the guard ring is arranged to provide RF isolation for the semiconductor mesa.

5 According to another aspect of the present invention, an integrated circuit comprises a semiconductor substrate, a buried insulation layer over the semiconductor substrate, a first semiconductor mesa over the buried insulation layer, a second semiconductor
10 mesa over the buried insulation layer, a first guard ring substantially surrounding the first semiconductor mesa, and a second guard ring substantially surrounding the second semiconductor mesa. The first guard ring is in contact with the semiconductor substrate, and the first
15 guard ring is arranged to provide RF isolation for the first semiconductor mesa. The second guard ring is in contact with the semiconductor substrate, and the second guard ring is arranged to provide RF isolation for the second semiconductor mesa.

20 According to still another aspect of the present invention, a method of isolating a semiconductor feature of an integrated circuit from RF signals comprises the following: forming a buried insulation layer over a semiconductor substrate; forming a

semiconductor feature in one or more semiconductor layers
so that the semiconductor feature is formed over a
portion of the buried insulation layer, wherein the
buried insulating layer has a trench therethrough down to
5 the semiconductor substrate that substantially encloses
the portion of the buried insulation layer, wherein the
one or more semiconductor layers has a trench
therethrough that substantially encloses the
semiconductor feature, and wherein the trench through the
10 one or more semiconductor layers substantially aligns
with the trench through the buried insulating layer;
and, filling the trench through the one or more
semiconductor layers and the trench through the buried
insulating layer with conducting material having low
15 resistivity so that a conductive guard ring substantially
surrounds the semiconductor feature.

According to yet another aspect of the present
invention, an integrated circuit comprises a
semiconductor substrate, a semiconductor feature, and a
20 guard ring. The semiconductor substrate forms a first
semiconductor layer. The semiconductor feature is formed
in a second semiconductor layer, and the second
semiconductor layer is over the first semiconductor
layer. The guard ring substantially surrounds the

semiconductor feature, the guard ring is in contact with the semiconductor substrate, and the guard ring is arranged to provide RF isolation for the semiconductor feature.

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Brief Description of the Drawings

These and other features and advantages of the present invention will become more apparent from a detailed consideration of the invention when taken in
10 conjunction with the drawings in which:

Figure 1 is a top plan view illustrating a semiconductor integrated circuit in accordance with the present invention;

Figure 2 is a sectional view illustrating the
15 semiconductor integrated circuit of Figure 1 taken along line 2-2;

Figure 3 is a sectional view illustrating the semiconductor integrated circuit of Figure 1 taken along line 3-3;

20 Figures 4-6 are sectional views illustrating a method of manufacturing the semiconductor integrated circuit as shown in Figure 2; and,

Figure 7 is a top view of an exemplary layout of an integrated circuit incorporating the present invention.

5 Detailed Description of the Invention

As shown in Figure 1, a semiconductor integrated circuit 10 in accordance with one embodiment of the present invention includes a single SOI substrate 12. The SOI substrate 12 typically includes a silicon
10 handle wafer, a buried oxide layer over the silicon handle wafer, and one or more silicon layers that are over the buried oxide layer and that are processed to form electronic devices of the integrated circuit. However, the present invention can be applied to non-SOI
15 substrates, such as bulk silicon, and to other SOI substrates, such as SOS (silicon-on-sapphire) substrates.

The SOI substrate 12 includes a first isolation guard ring 14 that isolates a first device mesa 16 and a second isolation guard ring 18 that isolates a second
20 device mesa 20. In addition, an optional first dielectric ring 22 may be provided between the first isolation guard ring 14 and the first device mesa 16, and an optional second dielectric ring 24 may be provided between the second isolation guard ring 18 and the second

device mesa 20. The dielectric in the first and second dielectric rings 22 and 24 may be silicon oxide or some other material, such as, for example, oxide/silicon nitride.

5 The first and second device mesas 16 and 20 may each comprise many different types of devices such as, for example, one or more transistors, and/or one or more diodes, and/or one or more capacitors, and/or one or more resistors, etc. Thus, any type of semiconductor element
10 or elements may be formed in each of the first and second device mesas 16 and 20. Thus, each of the first and second device mesas 16 and 20 may comprise one, two, or more such elements forming a single element or a sub-circuit. The semiconductor element or elements may be
15 active, passive, or a combination of both. Furthermore, any number of devices, device mesas, and isolation guard rings may be included on the SOI substrate 12.

 As shown in Figure 2, the SOI substrate 12 includes a silicon handle wafer 40 and a buried
20 insulating layer 42 that separates the first device mesa 16 from the silicon handle wafer 40. By way of example, the silicon handle wafer 40 may be formed of p- single crystal silicon, and the buried insulating layer 42 may be formed of a silicon oxide film. The silicon handle

wafer 40 is preferably a high resistivity (or high Z) substrate having a high ohm per centimeter rating such as, for example, 1 K Ω per centimeter. While a 1 K Ω per centimeter substrate performs very well, substrates
5 having other resistivities (or Z) such as 18 Ω per centimeter or above can be used.

The first isolation guard ring 14 surrounds the first device mesa 16. During formation of the first isolation guard ring 14, all of the layers (including any
10 shallow trench isolation oxide) above the buried insulation layer 42 and the buried insulation layer 42 selectively removed so as to form a trench that will be processed as described below in order to fabricate the first isolation guard ring 14.

15 The portion of the silicon handle wafer 40 that is exposed by the trench may be doped, such as by ion implantation. This doping improves to the ohmic contact between the first isolation guard ring 14 and the silicon handle wafer 40. The trench is filled with a low
20 resistivity material to form the first isolation guard ring 14. The low resistivity material, for example, may be a conductive metal such as tungsten, aluminum, or copper. However, conductive materials other than metals can be used for the low resistivity material. An

exemplary resistivity of such a low resistivity material is 5×10^{-3} Ohm-cm.

As shown in Figure 2, the first dielectric ring 22 may be formed down to the buried insulation layer 42.

5 The first isolation guard ring 14 surrounds the first device mesa 16, and the first isolation guard ring 14 also isolates the first device mesa 16 from a surrounding field n^- layer 44. One or more metal contacts 48 are applied to first isolation guard ring 14 to
10 provide a low resistance RF ground along one or more corresponding conductors 50. The one or more conductors 50 may be coupled to local ground through on-chip metal or, for better isolation, to an off-chip ground.

Accordingly, the first isolation guard ring 14
15 forms a low resistivity RF path to a metal layer which is connected to ground potential level.

As shown in Figures 1 and 3, the second isolation guard ring 18 surrounds the second device mesa 20. The second isolation guard ring 18 also contacts the
20 silicon handle wafer 40, and the silicon handle wafer 40 may be doped where it contacts the second isolation guard ring 18 so as to improve the ohmic contact between the second isolation guard ring 18 and the silicon handle wafer 40.

One or more metal contacts 62 are applied to the second isolation guard ring 18 to provide a low resistance RF ground along one or more corresponding conductors 64.

5 The first and second isolation guard rings 14 and 18 provide excellent RF isolation because electric fields created by RF power are terminated to ground through the first and second isolation guard rings 14 and 18 and the conductors 50 and 64. Having these RF
10 grounded terminations around the first and second device mesas 16 and 20 greatly improves RF isolation. Also, the use of the buried insulating layer 42 of the SOI substrate 12 provides additional RF isolation, and the use of the high resistivity (or high Z) silicon handle
15 wafer 40 of the SOI substrate 12 improves RF isolation by making the silicon handle wafer 40 a high resistance path for RF power. Any leaking RF power will prefer the path of least resistance which will not be the silicon handle wafer 40 if a high Z substrate is used therefor.

20 Furthermore, the present invention means that thin SOI can be used for advanced mixed (analog and digital) signal/RF CMOS technology. For example, the n-type layer 44 may be on the order of 0.16 micron instead of the 1 micron layer that is used in BiCMOS. Also, as

shown in Figures 2 and 3, the buried insulation layer 42 is completely removed in the trenches within which the first and second isolation guard rings 14 and 18 are formed to allow direct contact of the first and second isolation guard rings 14 and 18 to the silicon handle wafer 40 thus resulting in better RF isolation.

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Additionally, the material used to contact the silicon handle wafer 40 has a significantly lower resistivity than in prior devices resulting in better RF isolation.

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However, it should be noted that the present invention is not limited to the use of metals in the formation of the first and second isolation guard rings 14 and 18. Instead, in-situ doped low resistivity material/SEG (Selective Epitaxial Growth) can also be used to fill the

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trenches during formation of the first and second isolation guard rings 14 and 18.

The process for manufacturing the semiconductor integrated circuit 10 is shown in more detail in connection with Figures 4 to 6. As shown in Figure 4,

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the silicon handle wafer 40 is prepared by forming the buried insulating layer 42 over its main surface. The buried insulating layer 42 may be formed, for example, by high energy high dose ion implantation of oxygen into the silicon handle wafer 40. Alternatively, the buried

insulating layer 42 may be formed, for example, by using a bonded wafer process.

As shown in Figure 5, the n^- layer 44 is grown by epitaxial growth over the surface of the buried insulating layer 42. As shown in Figure 6, the trenches for the first isolation guard ring 14 and the first dielectric ring 22 are formed by anisotropic etching, such as, for example, by RIE. Specifically, the trench for the first isolation guard ring 14 extends from the main surface of the n^- layer 44 to the silicon handle wafer 40. The trench for the first dielectric ring 22 extends from the main surface of the n^- layer 44 to the buried insulating layer 42. A photoresist 70 may be used as a mask for the etching. Alternatively, a hard mask may be used as a mask for the etching in place of the photoresist 70.

After the photoresist 70 is removed, the trench for the first isolation guard ring 14 is filled with a conductive material such as, for example, metal, and the trench for the first dielectric ring 22 is filled with an insulator such as, for example, a silicon oxide. This insulator may be formed, for example, by depositing a silicon oxide film over the main surface of the n^- layer 44 by the CVD method and by etching back the silicon

oxide film. The silicon oxide film may be over-etched off except from the inside of the trench that is used to form the first dielectric ring 22. The trench that is used to form the first dielectric ring 22 could
5 alternatively be filled with other materials, such as, for example, oxide/silicon nitride.

Figure 7 is a top view of an exemplary layout of an integrated circuit 80. The integrated circuit 80 has two sub-circuits 82 and 84, although the integrated
10 circuit 80 may have additional sub-circuits (not shown). The sub-circuit 82, for example, may be a low noise amplifier and the sub-circuit 84, for example, may be a voltage controlled oscillator.

The sub-circuit 82 includes one or more device
15 mesas such as the device mesas 86, 88, and 90. The device mesa 86 is surrounded by an isolation guard ring 92, the device mesa 88 is surrounded by an isolation guard ring 94, and the device mesa 90 is surrounded by an isolation guard ring 96. The isolation guard rings 92,
20 94, and 96 may be arranged as shown in Figures 1-6 such that they contact corresponding doped areas of a semiconductor substrate 98 over which the integrated circuit 80 is formed. A chip metal 100 of the integrated

circuit 80 couples the isolation guard rings 92, 94, and 96 together and to a ground lead 102.

The sub-circuit 84 includes one or more device mesas such as the device mesas 104, 106, and 108. The
5 device mesa 104 is surrounded by an isolation guard ring 110, the device mesa 106 is surrounded by an isolation guard ring 112, and the device mesa 108 is surrounded by an isolation guard ring 114. The isolation guard rings 110, 112, and 114 also may be arranged as shown in
10 Figures 1-6 such that they contact corresponding doped areas of the semiconductor substrate 98 over which the integrated circuit 80 is formed. A chip metal 116 of the integrated circuit 80 couples the isolation guard rings 110, 112, and 114 together and to a ground lead 118.

15 The isolation guard rings 92, 94, and 96 may be considered to be a first isolation guard ring, and the isolation guard rings 110, 112, and 114 may be considered to be a second isolation guard ring. As seen in Figure 7, the integrated circuit 80 includes a third isolation
20 guard ring 120 that surrounds the sub-circuit 82 and that isolates the sub-circuit 82 from the sub-circuit 84. The third isolation guard ring 120 may be arranged as shown in Figures 1-6 such that its contacts a corresponding doped area of the semiconductor substrate 98 over which

the integrated circuit 80 is formed. A chip metal 122 of the integrated circuit 80 couples the third isolation guard ring 120 to a bond pad 124 that may be coupled to an off-chip ground.

5 Certain modifications of the present invention have been discussed above. Other modifications will occur to those practicing in the art of the present invention. For example, as described above, the silicon handle wafer 40 may be a p- silicon handle wafer, and the
10 layer 44 may be an n⁻ layer 44. However, other conductivity types may instead be used for these layers.

 Accordingly, the description of the present invention is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the
15 best mode of carrying out the invention. The details may be varied substantially without departing from the spirit of the invention, and the exclusive use of all modifications which are within the scope of the appended claims is reserved.

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